

# SN74ALS641A, SN74ALS642A, SN74AS641 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS300 – MARCH 1995

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Choice of True or Inverting Logic
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs

DEVICE	LOGIC
SN74ALS641A, SN74AS641	True
SN74ALS642A	Inverting

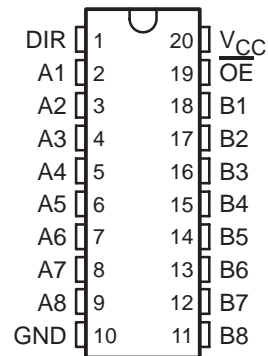
## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input disables the device so that the buses are effectively isolated.

The -1 versions of the SN74ALS641A and SN74ALS642A are identical to the standard versions, except that the recommended maximum  $I_{OL}$  is increased to 48 mA in the -1 versions.

The SN74ALS641A, SN74ALS642A, and SN74AS641 are characterized for operation from 0°C to 70°C.

DW OR N PACKAGE  
(TOP VIEW)



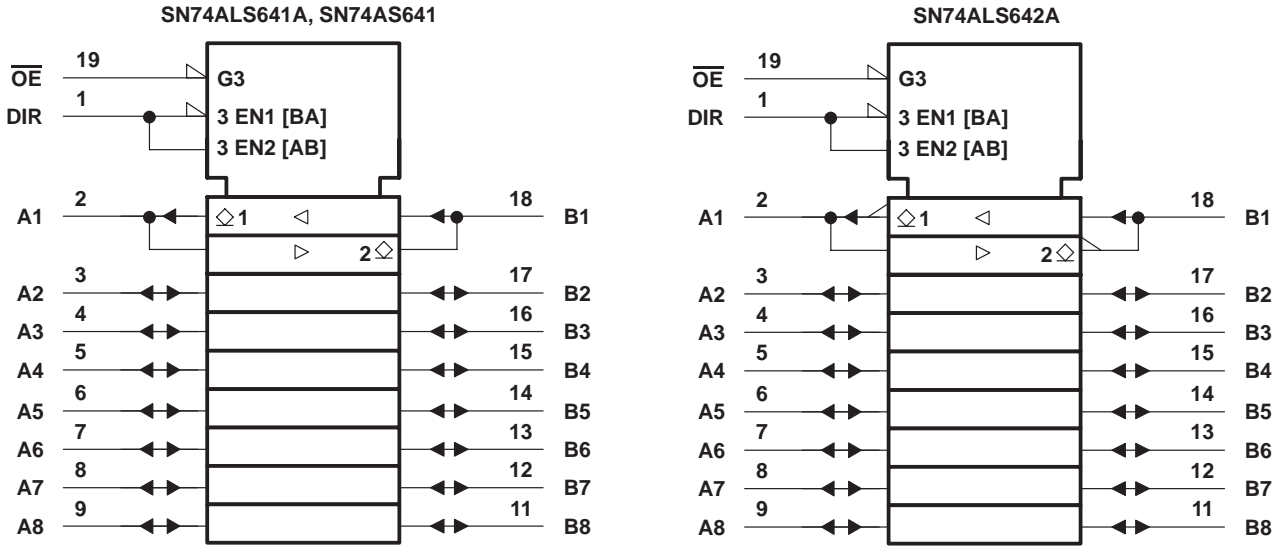
FUNCTION TABLE

INPUTS		OPERATION	
$\overline{OE}$	DIR	SN74ALS641A SN74AS641	SN74ALS642A
L	L	B data to A bus	$\overline{B}$ data to A bus
L	H	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

# SN74ALS641A, SN74ALS642A, SN74AS641 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS300 – MARCH 1995

## logic symbols†

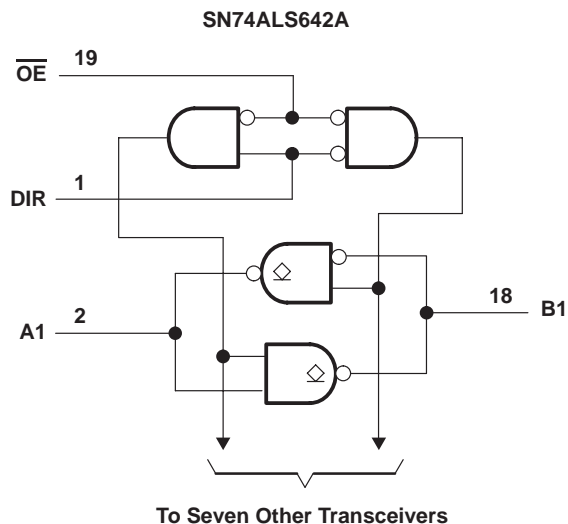
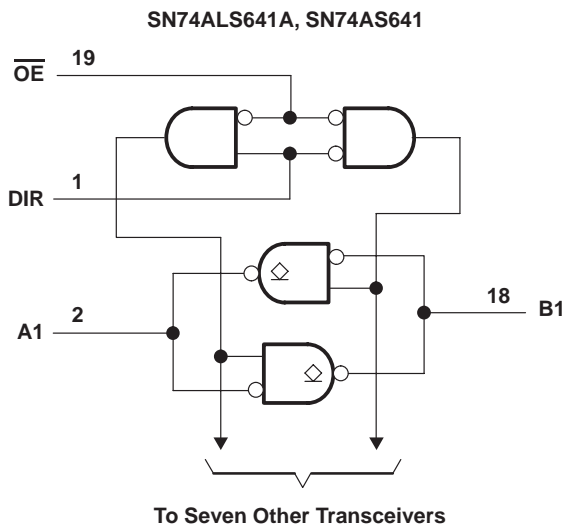


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN74ALS641A, SN74ALS642A, SN74AS641 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS300 – MARCH 1995

## logic diagrams (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ : All inputs and I/O ports	7 V
Operating free-air temperature range, $T_A$ : SN74ALS641A, SN74ALS642A	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN74ALS641A SN74ALS642A			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{OH}$	High-level output voltage			5.5	V
$I_{OL}$	Low-level output current			24	mA
				48‡	
$T_A$	Operating free-air temperature	0		70	°C

‡ Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V



# SN74ALS641A, SN74ALS642A, SN74AS641

## OCTAL BUS TRANSCEIVERS

### WITH OPEN-COLLECTOR OUTPUTS

SDAS300 – MARCH 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS641A SN74ALS642A			UNIT
				MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.5	V
$I_{OH}$		$V_{CC} = 4.5\text{ V}$ ,	$V_{OH} = 5.5\text{ V}$			0.1	mA
$V_{OL}$		$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$		0.25	0.4	V
			$I_{OL} = 24\text{ mA}$		0.35	0.5	
			$I_{OL} = 48\text{ mA}^\ddagger$		0.35	0.5	
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1	mA
$I_{IH}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	$\mu\text{A}$
	A or B ports§					20	
$I_{IL}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			-0.1	mA
	A or B ports§					-0.1	
$I_{CC}$	SN74ALS641A	$V_{CC} = 5.5\text{ V}$	Outputs high		25	37	mA
			Outputs low		33	47	
	SN74ALS642A	$V_{CC} = 5.5\text{ V}$	Outputs high		8	15	
			Outputs low		18	28	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Applies only to the -1 version and only if  $V_{CC}$  is between 4.75 V and 5.25 V

§ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

### switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 680\ \Omega$ , $T_A = \text{MIN to MAX}^\parallel$				UNIT
			SN74ALS641A		SN74ALS642A		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	5	25	10	30	ns
$t_{PHL}$			3	18	5	22	
$t_{PLH}$	$\overline{OE}$	A or B	8	30	10	30	ns
$t_{PHL}$			8	30	15	38	
$t_{PLH}$	DIR	A or B	8	32	10	30	ns
$t_{PHL}$			8	32	15	38	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



# SN74ALS641A, SN74ALS642A, SN74AS641 OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS300 – MARCH 1995

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ : All inputs and I/O ports .....	7 V
Operating free-air temperature range, $T_A$ : SN74AS641 .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN74AS641			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{OH}$	High-level output voltage			5.5	V
$I_{OL}$	Low-level output current			64	mA
$T_A$	Operating free-air temperature	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74AS641		UNIT
				MIN	TYP‡	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$		–1.2	V
$I_{OH}$		$V_{CC} = 4.5\text{ V}$ ,	$V_{OH} = 5.5\text{ V}$		0.1	mA
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 64\text{ mA}$	0.35	0.55	V
$I_I$	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$		0.1	mA
	A or B ports		$V_I = 5.5\text{ V}$		0.1	
$I_{IH}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$		20	µA
	A or B ports§				70	
$I_{IL}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$		–0.5	mA
	A or B ports§				–0.75	
$I_{CC}$		$V_{CC} = 5.5\text{ V}$	Outputs high	50	82	mA
			Outputs low	84	136	

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.



**SN74ALS641A, SN74ALS642A, SN74AS641**  
**OCTAL BUS TRANSCEIVERS**  
**WITH OPEN-COLLECTOR OUTPUTS**

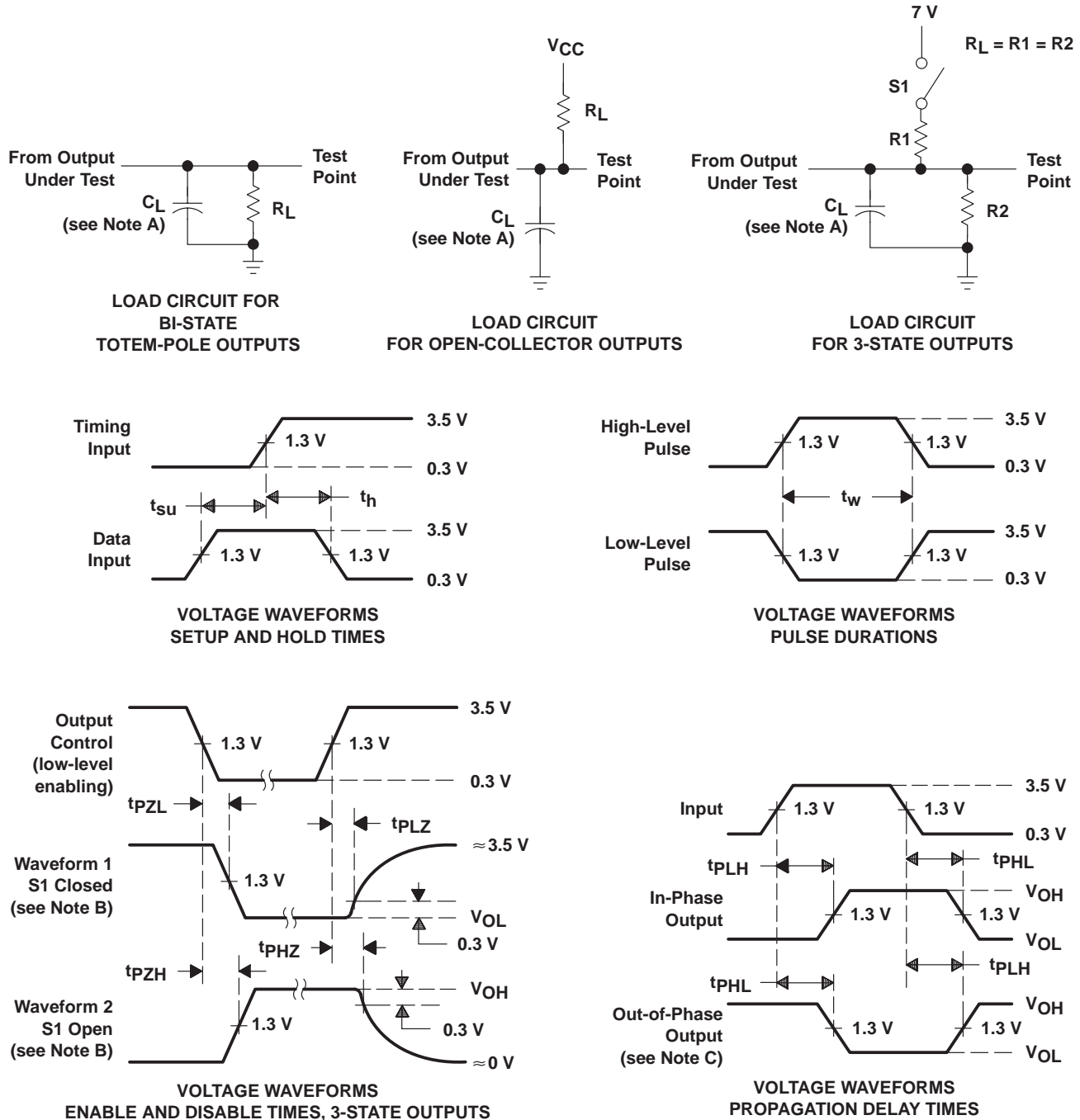
SDAS300 – MARCH 1995

**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 680 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74AS641		
			MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	5	21	ns
t <sub>PHL</sub>			1	7.5	
t <sub>PLH</sub>	$\overline{OE}$	A or B	5	21	ns
t <sub>PHL</sub>			1	9	
t <sub>PLH</sub>	DIR	A or B	5	22	ns
t <sub>PHL</sub>			1	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION  
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALS641A-1DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641A-1DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641A-1DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641A-1DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641A-1DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641A-1DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641A-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS641A-1NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS641A-1NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641A-1NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641A-1NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS641ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS641ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS641ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642A-1DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642A-1DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642A-1DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALS642A-1DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642A-1DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642A-1DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642A-1N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS642A-1NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS642A-1NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642A-1NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642A-1NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS642ADW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74ALS642ADWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74ALS642AN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74AS641DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS641DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS641DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS641DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS641DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS641DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS641N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS641NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS641A-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS641A-1NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74ALS641ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS641ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74ALS642A-1DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS642A-1NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74AS641DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS641A-1DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS641A-1NSR	SO	NS	20	2000	346.0	346.0	41.0
SN74ALS641ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS641ANSR	SO	NS	20	2000	346.0	346.0	41.0
SN74ALS642A-1DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ALS642A-1NSR	SO	NS	20	2000	346.0	346.0	41.0
SN74AS641DWR	SOIC	DW	20	2000	346.0	346.0	41.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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